IN THE SPECIFICATION

Please amend Paragraph 49 as follows:

[49] Each bit line (BL and BLC) further includes an additional pair of transistors 208 and 210 connected to a bit line load (BLLOAD) and bit line force (FORCEBL) signal, respectively. The first of these transistors 208 is a p-channel device connecting the bit line to Vcc/Vdd. The BLLOAD signal is connected to the gate of each p-channel device 208. The second of these transistors 210 is an n-channel device connecting the bit line to ground. The FORCEBL signal is connected to the gate of each n-channel device 210. Once each of the word lines has been activated using charge sharing followed by Vcc/Vdd pull up, BLLOAD is driven high by the tamper detection circuit and FORCEBL is driven high ~~low~~. This disconnects the bit lines from Vcc ~~/Vdd~~ and drives both BL and BLC in each memory cell to ground to effectuate a destruction of the data stored in the latch.